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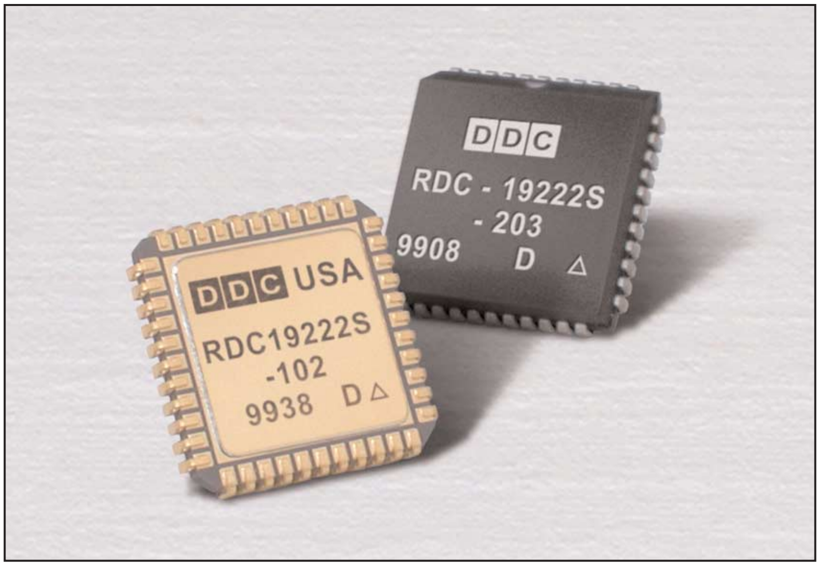
# RDC-19220/2S
# 16-BIT MONOLITHIC TRACKING RESOLVER-TO-DIGITAL (R/D) CONVERTER




## DESCRIPTION

The RDC-19220/2S is a low-cost, versatile, state-of-the-art 16-bit monolithic Resolver-to-Digital (R/D) Converter. This single chip converter offers programmable features such as resolution, bandwidth and velocity output scaling.

Resolution programming allows selection of 10, 12, 14, or 16 bits, with accuracies to 1.3 minutes. This feature combines the high tracking rate of a 10-bit converter with the precision and low-speed velocity resolution of a 16-bit converter in one package.

The internal Synthesized Reference section eliminates errors due to quadrature voltage. Previously, a 6 degree phase shift caused problems for a 16-bit converter. The synthesized reference capability ensures operation with a phase shift up to 45 degrees. The velocity output (VEL) from the RDC-19220/2S, which can be used to replace a tachometer, is a 4 V signal referenced to ground. The full-scale value of VEL is set by the user with a single resistor.

The RDC-19220/2S converter is available with operating temperature ranges of 0° to +70°C, -40° to +85°C, and -55° to +125°C.

## APPLICATIONS

The low cost, small size, high accuracy, and versatile performance of the RDC-19220/2S converter makes it ideal for use in modern high performance industrial control systems. Typical applications include motor control, radar antenna positioning, machine tool control, robotics, and process control. Class K and MIL-PRF-38534 processing is available for space and military applications.

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## FEATURES

- Accuracy up to 1.3 Arc Minutes
- Internal Synthesized Reference
- +5 Volt Only Option
- Programmable:
  - Resolution: 10-, 12-, 14-, or 16-Bit
  - Bandwidth
  - Tracking Rate
- Differential Resolver Input Mode
- Velocity Output Eliminates Tachometer
- Built-In-Test ($\overline{\text{BIT}}$) Output, No 180° Hangup
- -55° to +125°C Operating Temperature
- Class K and MIL-PRF-38534 Options

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7382

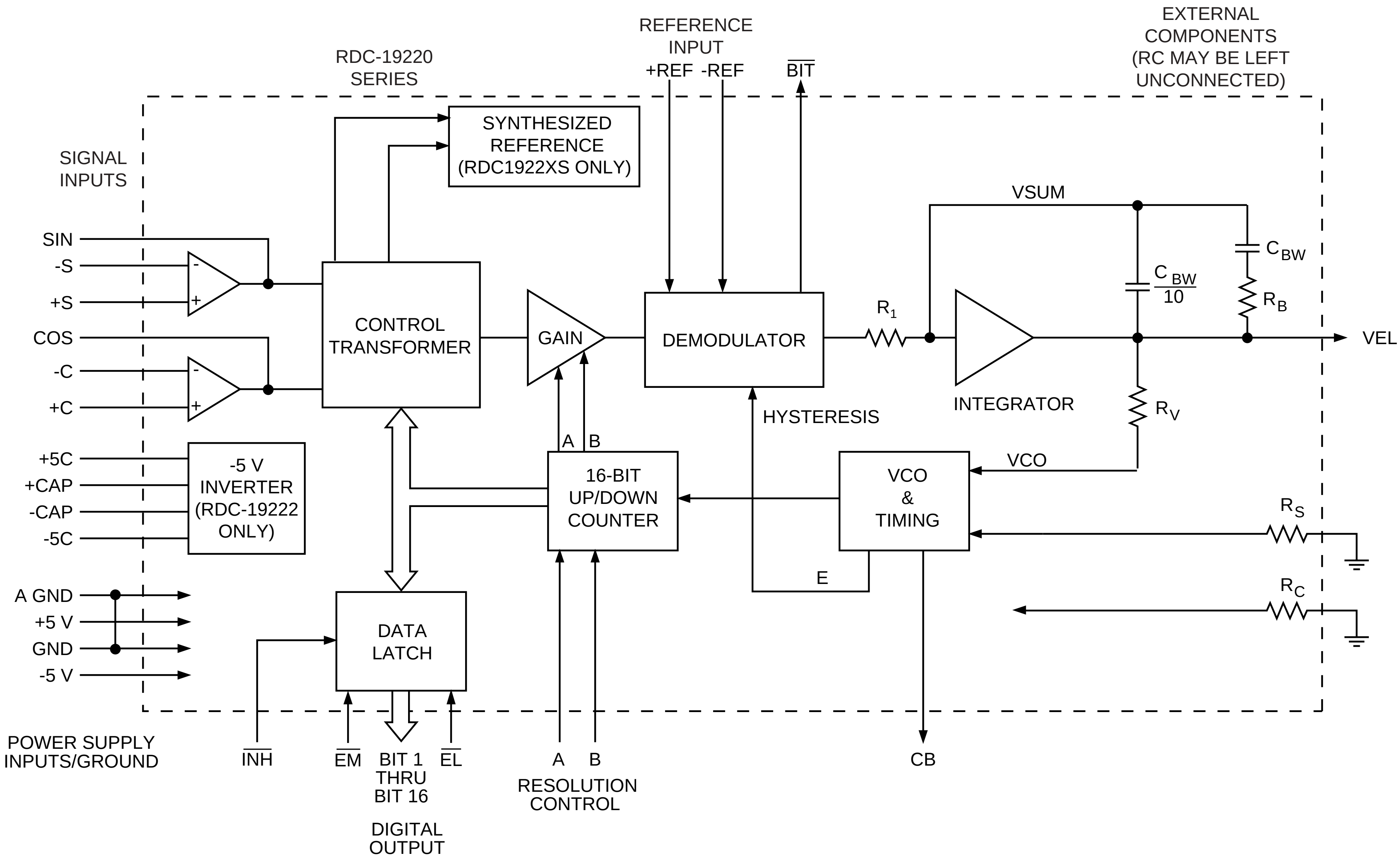



**FIGURE 1. RDC-19220/2S BLOCK DIAGRAM**

## TABLE 1. RDC-19220/2S SPECIFICATIONS

**These specifications apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation & 10% harmonic distortion.**

| PARAMETER | UNIT | VALUE | | |
|---|---|---|---|---|
| **RESOLUTION** | Bits | 10, 12, 14, or 16 (notes 1 & 2) | | |
| **FREQUENCY RANGE** | Hz | 47-1k (note 4) | 1k - 4k | 4k - 10k |
| **ACCURACY -XX2** | Min | 4 +1 LSB | 4 +1 LSB | 5 +1 LSB |
| **-XX3** (NOTE 3) | Min | 2 +1 LSB | 2 +1 LSB | 3 +1 LSB |
| Repeatability | LSB | ± 1 | ± 1 | ± 2 |
| Differential Linearity | LSB | ± 1 | ± 1 | ± 2 |
| **FREQUENCY RANGE** | Hz | 47-1k (note 4) | 1k - 5k (note 8) | |
| **ACCURACY -XX5** (NOTE 3) | Min | 1 +1 LSB | 1 +1 LSB | |
| Repeatability | LSB | ± 1 | ± 1 | |
| Differential Linearity | LSB | ± 1 | ± 1 | |
| **REFERENCE** | | (+REF, -REF) | | |
| Type | | Differential | | |
| Voltage: differential | V | ±10 max (note 9) | | |
| single ended | V | ±5 max (note 9) | | |
| overload | V | ±25 continuous 100 transient | | |
| Frequency | Hz | DC to 10,000 (note 8) | | |
| Input Impedance | Ohm | 10M min //20 pf | | |
| ±Sig/Ref Phase Shift | deg | 45 max from 400 Hz to 10 kHz (note 5) | | |
| **SIGNAL INPUT** | | (+S, -S, SIN, +C, -C, COS) | | |
| Type | | Resolver, differential, groundbased | | |
| Voltage: operating | Vrms | 2 ±15% | | |
| overload | V | ±25 continuous | | |
| Input Impedance | Ohm | 10M min //10 pf. | | |
| **DIGITAL INPUT/OUTPUT** | | | | |
| Logic Type | | TTL/CMOS compatible | | |
| Inputs | | Logic 0 = 0.8 V max. / Logic 1 = 2.0 V min.<br>Loading=10 µA max P.U. current source to +5 V //5 pF max., CMOS transient protected | | |
| Inhibit ($\overline{\text{INH}}$) | | Logic 0 inhibits; Data stable within 0.1 µS | | |
| Enable Bits 1 to 8 ($\overline{\text{EM}}$) | | Logic 0 enables; Data stable within 150 nS | | |
| Enable Bits 9 to 16 ($\overline{\text{EL}}$) | | Logic 1 = High Impedance, Data High Z within 100 nS | | |
| Resolution and Mode Control (A & B)<br>(see notes 1 and 2) | | <table><tr><th>Mode</th><th>B</th><th>A</th><th>Resolution</th></tr><tr><td>Resolver</td><td>0</td><td>0</td><td>10 bits</td></tr><tr><td>“</td><td>0</td><td>1</td><td>12 bits</td></tr><tr><td>“</td><td>1</td><td>0</td><td>14 bits</td></tr><tr><td>“</td><td>1</td><td>1</td><td>16 bits</td></tr><tr><td>LVDT</td><td>-5 V</td><td>0</td><td>8 bits</td></tr><tr><td>“</td><td>0</td><td>-5 V</td><td>10 bits</td></tr><tr><td>“</td><td>1</td><td>-5 V</td><td>12 bits</td></tr><tr><td>“</td><td>-5 V</td><td>-5 V</td><td>14 bits</td></tr></table> | | |
| Outputs | | | | |
| Parallel Data (1-16) | | 10, 12, 14 or 16 parallel lines; natural binary angle positive logic (see note 2) | | |
| Converter Busy (CB) | | 0.25 to 0.75 µs positive pulse leading edge initiates counter update. | | |
| Built-in-Test ($\overline{\text{BIT}}$) | | Logic 0 for $\overline{\text{BIT}}$ condition.<br>±100 LSBs of error with a filter of 500 µS total, Loss-of-Signal (LOS) less than 500 mV, or Loss-of-Reference (LOR) less than 500 mV. | | |
| Drive Capability | | 50 pF+<br>Logic 0; 1 TTL load, 1.6 mA at 0.4 V max.<br>Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min<br>Logic 0; 100 mV max driving CMOS<br>Logic 1; +5 V supply minus 100 mV min driving CMOS High Z; 10 uA //5 pF max | | |

Notes:
1. Unused data bits are set to logic “0.”
2. In LVDT mode, bit 16 is LSB for 14-bit resolution or bit 12 is LSB for 10-bit resolution
3. Accuracy in LVDT mode is 0.15% + 1 LSB of full scale.
4. If the frequency is between 47Hz and 1kHz, then there may be 1 LSB of jitter at quadrant boundaries.
5. The maximum phase shift tolerance will degrade linearly from 45 degrees at 400 Hz to 30 degrees at 60 Hz.
6. See text, General Setup Considerations.
7. When using internally generated -5V the internal -5V charge pump when measured at the converter pin, may be as low as -20% (or -4V).
8. -XX5 accuracy is 1minute + 1 LSB up to 5 kHz max.
9. A signal less than 500 mV will assert BIT.

| TABLE 1. RDC-19220/2S SPECIFICATIONS (CONT.) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **UNIT** | **VALUE** | | | |
| **DYNAMIC CHARACTERISTICS** | | (at maximum bandwidth) | | | |
| Resolution | bits | 10 | 12 | 14 | 16 |
| Tracking Rate-min (note 6) | rps | 1152 | 288 | 72 | 18 |
| Bandwidth(Closed Loop) Max | Hz | 1200 | 1200 | 600 | 300 |
| Ka | $1/sec^2$ | 5.7M | 5.7M | 1.4M | 360k |
| A1 | 1/sec | 19.5 | 19.5 | 4.9 | 1.2 |
| A2 | 1/sec | 295k | 295k | 295k | 295k |
| A | 1/sec | 2400 | 2400 | 1200 | 600 |
| B | 1/sec | 1200 | 1200 | 600 | 300 |
| Acceleration (1 LSB lag) | $deg/s^2$ | 2M | 500k | 30k | 2k |
| Settling Time(179° step) | msec | 2 | 8 | 20 | 50 |
| **VELOCITY CHARACTERISTICS** | | | | | |
| Polarity | | Positive for increasing angle | | | |
| Voltage Range(Full Scale) | V | ±4 (at nominal ps) | | | |
| Scale Factor Error | % | 10 typ | 20 max | | |
| Scale Factor TC | PPM/C | 100 typ | 200 max | | |
| Reversal Error | % | 0.75 typ | 1.3 max | | |
| Linearity | % | 0.25 typ | 0.50 max | | |
| Zero Offset | mV | 5 typ | 10 max | | |
| Zero Offset TC | µV/C | 15 typ | 30 max | | |
| Load | kΩ | | 8 max | | |
| Noise | Vp/V | 1 typ | 0.125 min, 2 max | | |
| **POWER SUPPLIES** | | (notes 6 and 7) | | | |
| Nominal Voltage | V | +5 | -5 | | |
| Voltage Range | % | ±5 | ±5 | | |
| Max Volt. w/o Damage | V | +7 | -7 | | |
| Current | mA | 14 typ, 22 max (each) | | | |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | | | | |
| -30X | °C | 0 to +70 | | | |
| -20X | °C | -40 to +85 | | | |
| -10X | °C | -55 to +125 | | | |
| Storage | °C | -65 to +150 | | | |
| **THERMAL RESISTANCE** | | | | | |
| Junction to Case, θjc | | | | | |
| 40-Pin DDIP (Ceramic) | °C/W | 4.6 | | | |
| 44-Pin J-Lead (Plastic) | °C/W | 72.6 | | | |
| 44-Pin J-Lead (Ceramic) | °C/W | 2.4 | | | |
| **PHYSICAL CHARACTERISTICS** | | | | | |
| Size: 40-pin DDIP | in(mm) | 2.0 x 0.6 x 0.2 (50.8 x 15.24 x 5.08) | | | |
| 44-pin J-lead | in(mm) | 0.690 square (17.526) | | | |
| Weight: | | Plastic | Ceramic | | |
| 40-pin DDIP | oz (g) | N/A | 0.24 (6.80) | | |
| 44-pin J-lead | oz (g) | 0.08 (2.27) | 0.064 (1.84) | | |

## THEORY OF OPERATION

The RDC-19220/2S series of converter is a single CMOS custom monolithic chip. It is implemented using mixed signal CMOS technology which merges precision analog circuitry with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

FIGURE 1 is the RDC-19220/2S Functional Block Diagram. The converter operates with ±5 V DC power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of two main sections; a converter and a digital interface. The converter front-end consists of sine and cosine differential input amplifiers. These inputs are protected to ±25 V with 2 kΩ resistors and diode clamps to the ±5 V DC supplies. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16-bit digital angle $\phi$. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

**Note:** The transfer function of the CT is normally trigonometric, but in LVDT mode the transfer function is triangular (linear) and could thereby convert any linear transducer output.

The converter accuracy is limited by the precision of the computing elements in the CT. For enhanced accuracy, the CT in these converters use capacitors in precision ratios, instead of the more conventional precision resistor ratios. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate (70 kHz) to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage-controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and a lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

## TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and its Bode Plots (open and closed loop). These are shown in FIGURES 2, 3, and 4.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where: A is the gain coefficient
$A^2 = A_1A_2$
B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod with 2 Vrms input)
- Integrator gain = $\frac{C_SF_S}{1.1C_{BW}}$ volts per second per volt
- VCO Gain = $\frac{1}{1.25\,R_VC_{VCO}}$ LSBs per second per volt

where: $C_S$ = 10 pF
$F_S$ = 70 kHz when Rs = 30 kΩ
$F_S$ = 100 kHz when Rs = 20 kΩ
$F_S$ = 125 kHz when Rs = 15 kΩ
$C_{VCO}$ = 50 pF

$R_V$, $R_B$, and $C_{BW}$ are selected by the user to set velocity scaling and bandwidth.

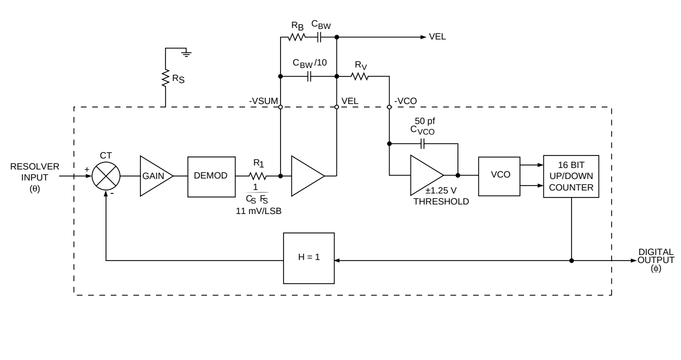



**FIGURE 2. TRANSFER FUNCTION BLOCK DIAGRAM #1**

## GENERAL SETUP CONDITIONS

DDC has external component selection software which considers all the criteria below and, in a simple fashion, asks the key parameters (carrier frequency, resolution, bandwidth, and tracking rate) to derive the external component values.

The following recommendations should be considered when installing the RDC-19220/2S Resolver-to-Digital (R/D) converter:

1) When setting the bandwidth (BW) and Tracking Rate (TR) (selecting five external components), the system requirements need to be considered. For the greatest noise immunity, select the minimum BW and TR the system will allow.

2) Power supplies are ±5V DC. For lowest noise performance it is recommended that a 0.1µF or larger cap be connected from each supply to ground near the converter package.

3) Resolver inputs and velocity output are referenced to AGND. This pin should be connected to GND near the converter package. Digital currents flowing through ground will not disturb the analog signals.

4) The $\overline{\text{BIT}}$ output, which is active low, is activated by an error of approximately 100 LSBs. During normal operation, for step inputs or on power up, a large error can exist.

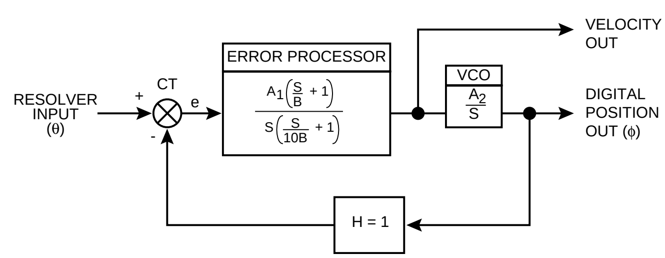



**FIGURE 3. TRANSFER FUNCTION BLOCK DIAGRAM #2**

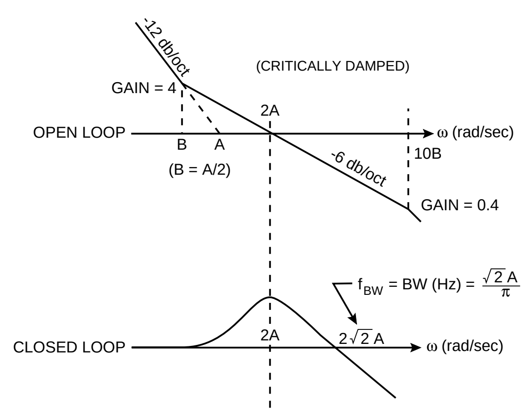



**FIGURE 4. BODE PLOTS**

5) Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

- Select the desired $f_{BW}$ (closed loop), based on overall system dynamics.
- Select fcarrier $\geq 3.5\ f_{BW}$
- Compute $R_V = 55\ k\Omega \times \dfrac{\{\text{For the converter max tracking rate value, see the row indicated in TABLE 3.}\}}{\text{Application max rate}}$
- Compute $C_{BW}\ (pF) = \dfrac{3.2 \times F_S\ (Hz) \times 10^8}{R_V \times (f_{BW})^2}$
- Where FS = 70 kHz for $R_S = 30\ k\Omega$
  100 kHz for $R_S = 20\ k\Omega$
  125 kHz for $R_S = 15\ k\Omega$
- Compute $R_B = \dfrac{0.9}{C_{BW} \times f_{BW}}$
- Compute $\dfrac{C_{BW}}{10}$

6) Selecting a $f_{BW}$ that is too low relative to the maximum application tracking rate can create a spin-around condition in which the converter never settles. The relationship to insure against spin-around is as follows (TABLE 2.):

**TABLE 2. TRACKING/BW RELATIONSHIP**

| RPS (MAX)/BW | RESOLUTION |
|---|---|
| 1 | 10 |
| 0.50 | 12 |
| 0.25 | 14 |
| 0.125 | 16 |

7) **RDC-19222 package only:**
When using the built-in -5 V inverter connect as shown:

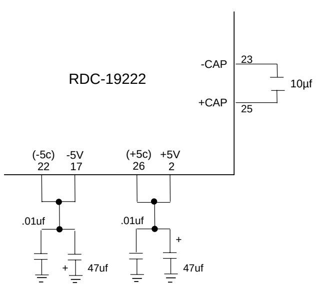



**FIGURE 5. -5V BUILT-IN INVERTER**

The current drain from the +5 V supply doubles. No external -5 V supply is needed. The power supply 47µf caps shown may be substituted with 10µf caps if the P/S lines are clean (min noise).

When using the built-in -5 V inverter, the maximum tracking rate should be scaled for a velocity output of 3.5 V max. Use the following equation to determine tracking rate used in the formula in Step 5:

$$\frac{\text{TR (required)} \times (4.0)}{(3.5)} = \text{Tracking rate used in calculation}$$

Note: When using the highest BW and Tracking Rates, use of the -5 V inverter is not recommended.

## HIGHER TRACKING RATES AND CARRIER FREQUENCIES

Tracking rate (nominally 4 V) is limited by two factors: velocity voltage saturation and maximum internal clock rate (nominally 1,333,333 Hz). An understanding of their interaction is essential to extending performance.

The General Setup Considerations section makes note of the selection of Rv for the desired velocity scaling. Rv is the input resistor to an inverting integrator with a 50 pF nominal feedback capacitor. When it integrates to -1.25 V, the converter counts up 1 LSB and when it integrates to +1.25 V, the converter counts down 1 LSB. When a count is taken, a charge is dumped on the capacitor such that the voltage on it changes 1.25 V in a direction to bring it to 0 V. The output counts per second per volt input is therefore:

$$\frac{1}{(R_V \times 50\ pF \times 1.25)}$$

As an example:

Calculate Rv for the maximum counting rate, at a VEL voltage of 4 V.

For a 12-bit converter there are $2^{12}$ or 4096 counts per rotation. 1,333,333/4096 = 325 rotations per second or 333,333 counts per second per volt.

$$R_V = \frac{1}{(333{,}333 \times 50\ pF \times 1.25)} = 48k\ Ohms$$

The maximum rate capability of the RDC-19220/2S is set by $R_S$.

When $R_S$ = 30 kHz it is nominally 1,333,333 counts/second, which equates to 325 rps (rotations per second). This is the absolute maximum; it is recommended to only run at < 90% of this rate (as given in TABLE 3), therefore the minimum $R_V$ will be limited to 55 kOhms.

**TABLE 3. MAX TRACKING RATE (MIN) IN RPS**

| $R_C$ | $R_S$ | RESOLUTION | | | |
|---|---|---|---|---|---|
| | | 10 | 12 | 14 | 16 |
| 30k or open* | 30 k | 1152 | 288 | 72 | 18 |

Depending on the resolution, select one of the values from this row, for use in converter max tracking rate formula. (See formula in Step 5.)

Carrier frequency is shown in TABLE 4.

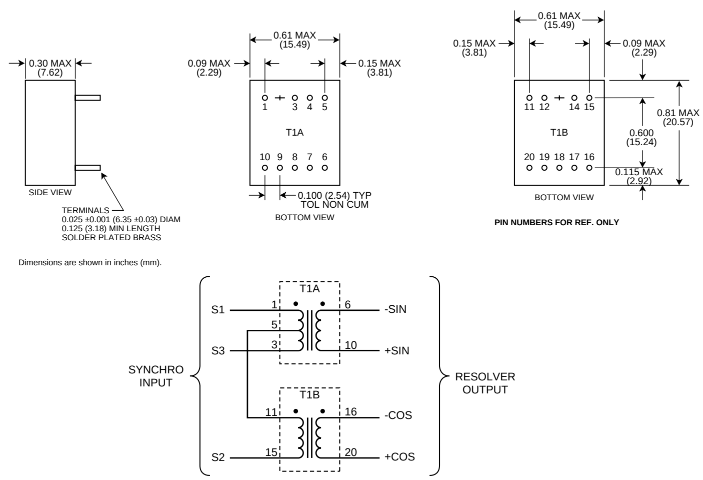
**TABLE 4. CARRIER FREQUENCY (MAX) IN KHZ**

| $R_C$ | $R_S$ | RESOLUTION | | | |
|---|---|---|---|---|---|
| | | 10 | 12 | 14 | 16 |
| 30k or open* | 30 k | 10 | 10 | 5 | 5 |

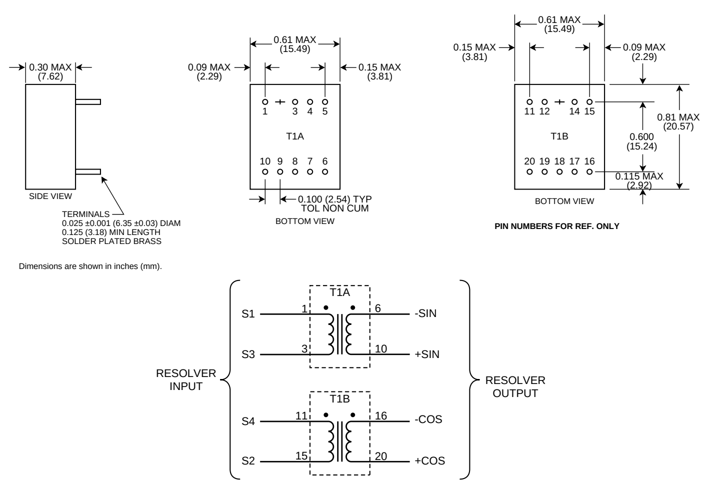
*The use of a high quality thin-film resistor will provide better temperature stability than leaving open.

| TABLE 5. TRANSFORMERS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| P/N | TYPE | FREQUENCY (HZ)* | IN (VRMS)* | OUT (VRMS)** | ANGLE ACCURACY*** | LENGTH (IN) | WIDTH (IN) | HEIGHT (IN) | FIGURE NUMBER |
| 52034 | S - R | 400 | 11.8 | 2 | 1 | 0.81 | 0.61 | 0.3 | 6A |
| 52035 | S - R | 400 | 90 | 2 | 1 | 0.81 | 0.61 | 0.3 | 6A |
| 52036 | R - R | 400 | 11.8 | 2 | 1 | 0.81 | 0.61 | 0.3 | 6B |
| 52037 | R - R | 400 | 26 | 2 | 1 | 0.81 | 0.61 | 0.3 | 6B |
| 52038 | R - R | 400 | 90 | 2 | 1 | 0.81 | 0.61 | 0.3 | 6B |
| B-426 | Reference | 400 | 115 | 3.4 | N/A | 0.81 | 0.61 | 0.32 | 6C |
| 52039-X | Synchro | 60 | 90 | 2 | 1 | 1.1 | 1.14 | .42 | 6D |
| 24133-X | Reference | 60 | 115 | 3/6 **** | N/A | 1.125 | 1.125 | .42 | 6D |

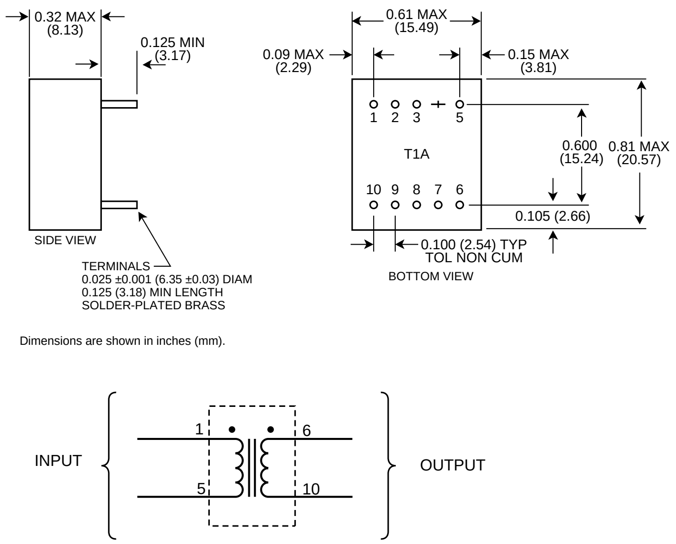
* ±10% Frequency (Hz) and Line-to-Line input voltage (Vrms) tolerances
** 2 Vrms Output Magnitudes are -2 Vrms ±0.5% full scale
*** Angle Accuracy (Max Minutes)
**** 3 Vrms to ground or 6 Vrms differential (±3% full scale)
Dimensions are for each individual main and teaser
60 Hz Synchro transformers are active (requires ±15 Vdc power supplies)
400 Hz transformer temperature range: -55°C to +125°C
60 Hz transformer (52039-X, 24133-X) temperature ranges: add to part number -1 or -3,
-1 = -55°C to +85°C
-3 = 0 to +70°C



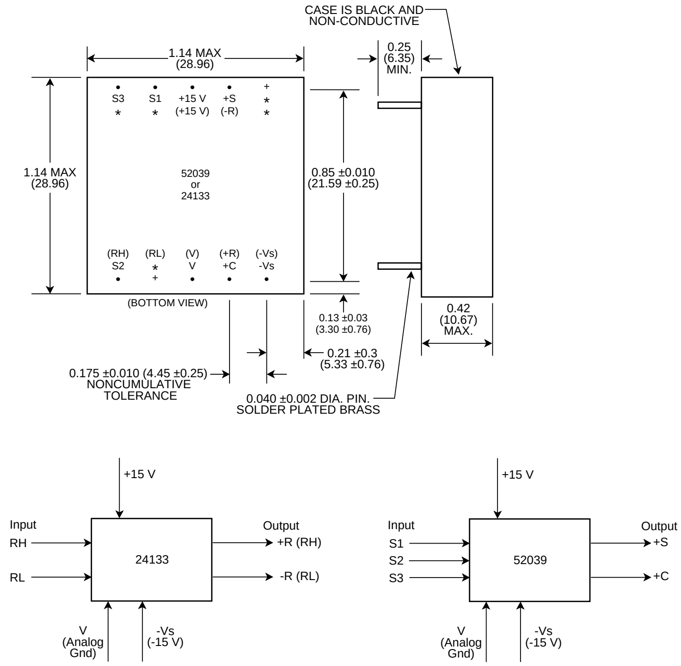

## FIGURE 6A. TRANSFORMER LAYOUT AND SCHEMATIC (SYNCHRO INPUT - 52034/52035)




## FIGURE 6B. TRANSFORMER LAYOUT AND SCHEMATIC (RESOLVER INPUT - 52036/52037/52038)

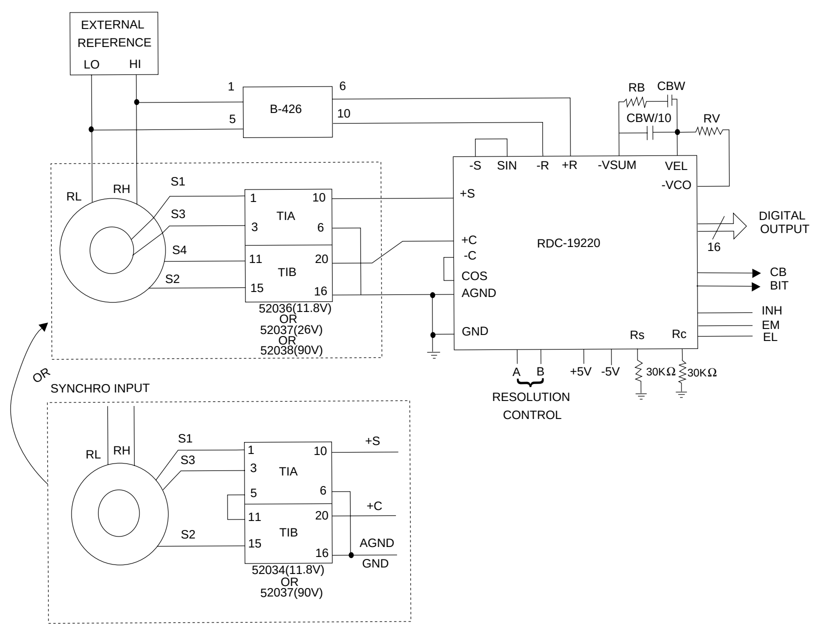



## FIGURE 6C. TRANSFORMER LAYOUT AND SCHEMATIC (REFERENCE INPUT - B-426)




The mechanical outline is the same for the synchro input transformer (52039) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ). An asterisk * indicates that the pin is omitted.

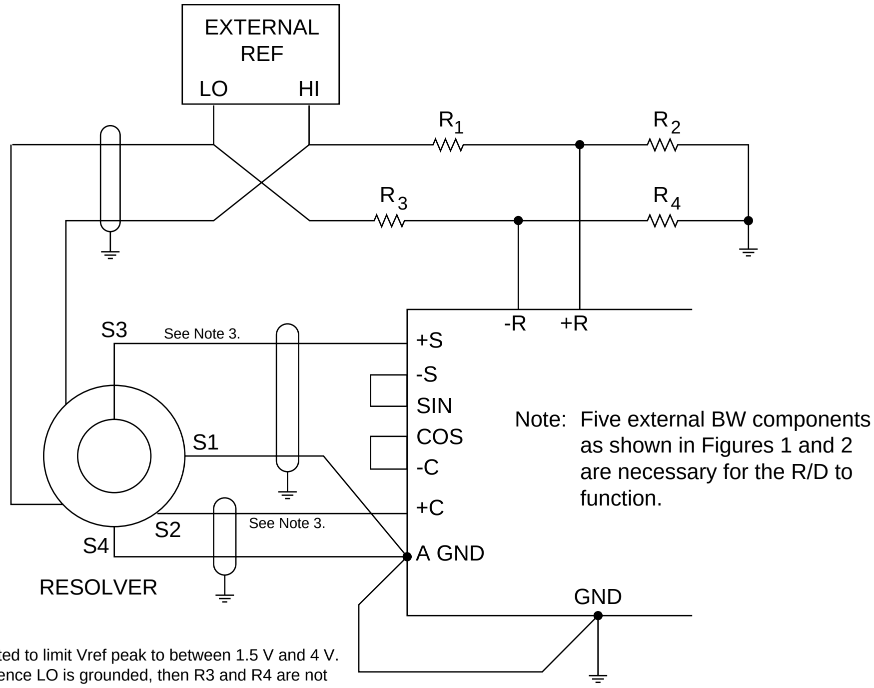
## FIGURE 6D. 60 HZ SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS (SYNCHRO INPUT - 52039 / REFERENCE INPUT - 24133)




## FIGURE 7. TYPICAL TRANSFORMER CONNECTIONS

## TYPICAL INPUTS

FIGURES 8 through 10 illustrate typical input configurations




Notes:
1) Resistors selected to limit Vref peak to between 1.5 V and 4 V.
2) If external reference LO is grounded, then R3 and R4 are not needed, and -R is connected to GND.
3) 10k ohms, 1 % series current limit resistors are recommended.

**FIGURE 8. TYPICAL CONNECTIONS, 2 VOLT RESOLVER, DIRECT INPUT**

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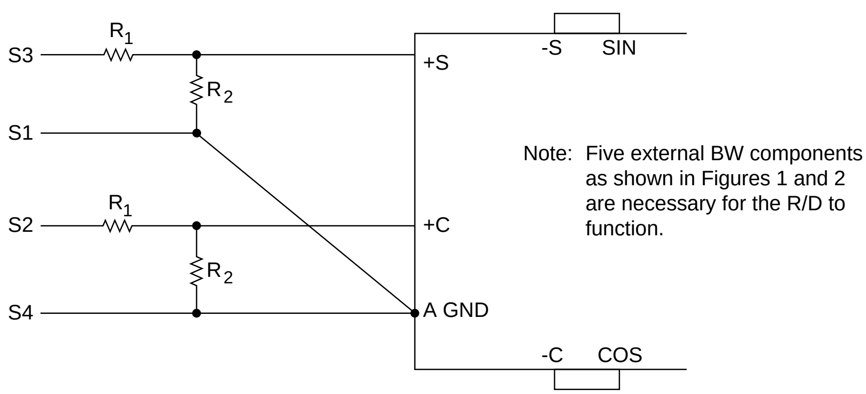
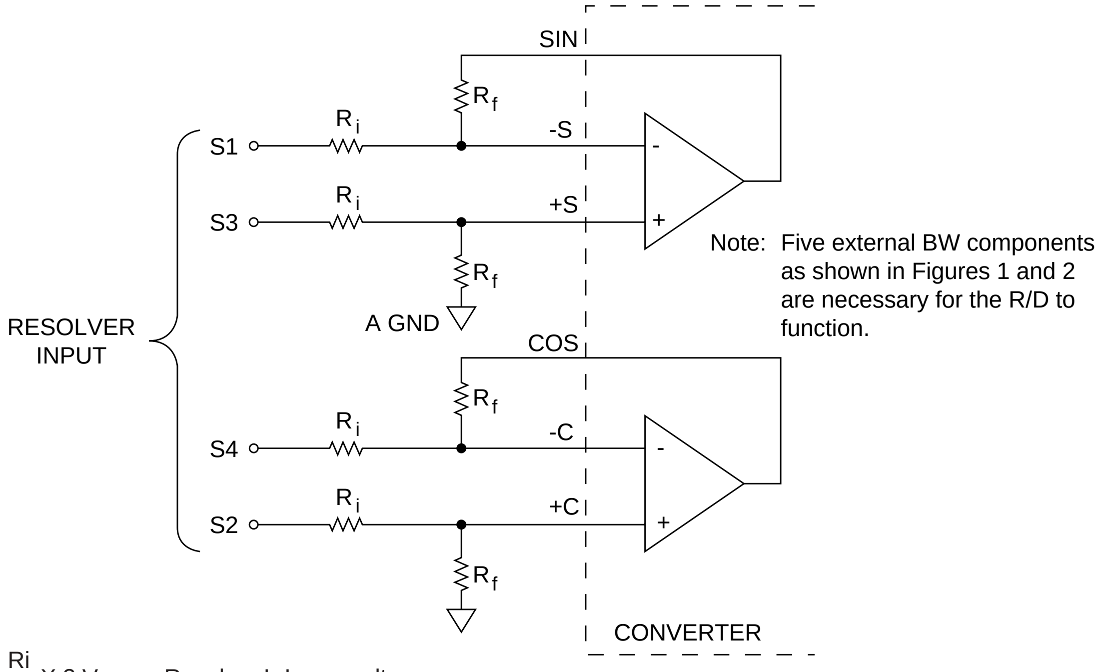



$$\frac{R2}{R1 + R2} = \frac{2}{X\ \text{Volt}}$$

R1 + R2 should not load the Resolver too much; it is recommended that R2 = 10k.

R1 + R2 Ratio Errors will result in Angular Errors,
2 cycle, 0.1% Ratio Error = 0.029˚ Peak Error.

**FIGURE 9. TYPICAL CONNECTIONS, X-VOLT RESOLVER, DIRECT INPUT**

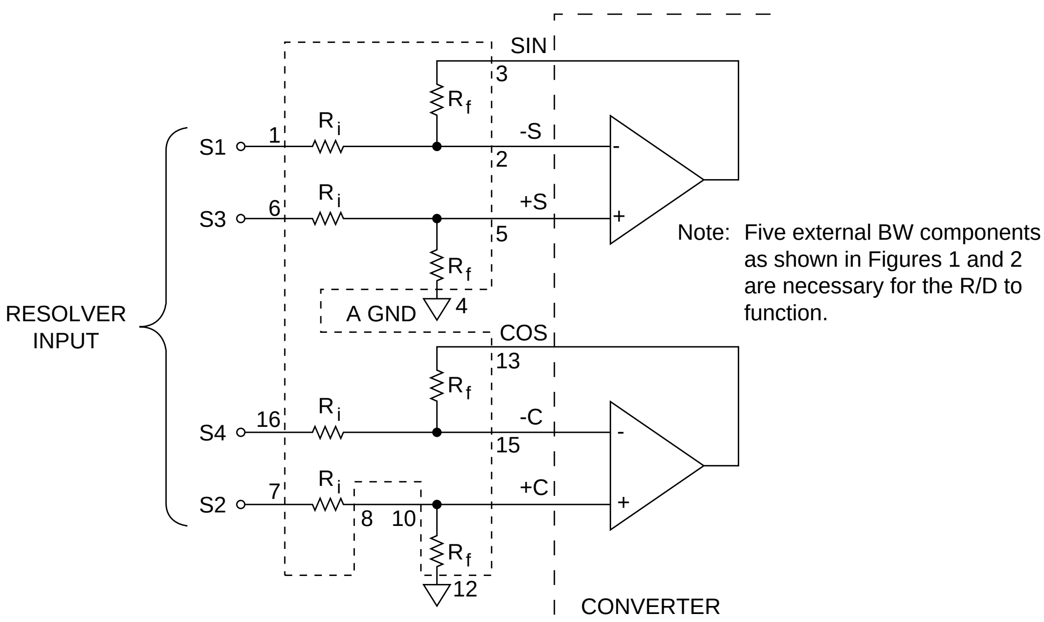



$\frac{Ri}{Rf}$ X 2 Vrms = Resolver L-L rms voltage

Rf ≥ 6 kΩ

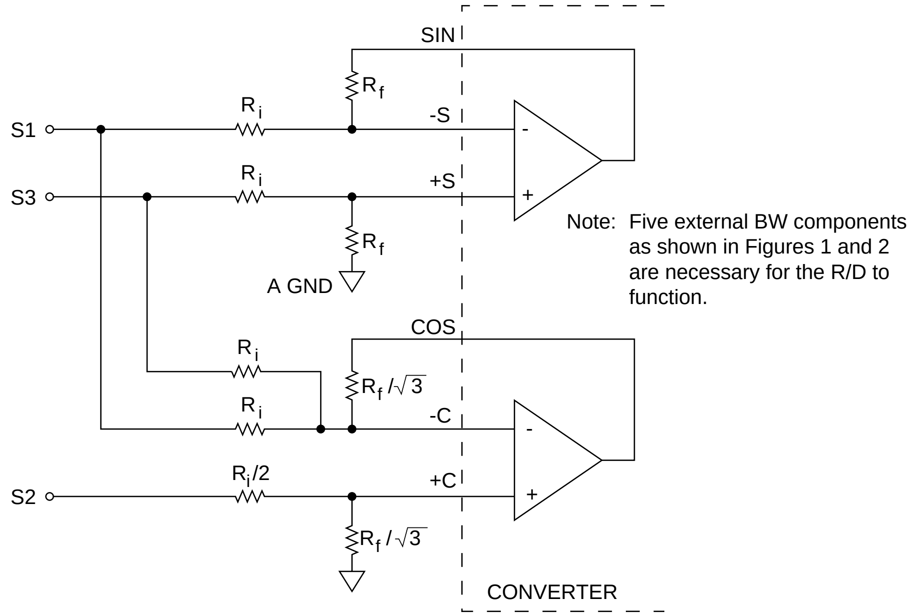
S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to AGND at the converter.

**FIGURE 10A. DIFFERENTIAL RESOLVER INPUT**




S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to AGND at the converter.
For DDC-49530: Ri = 70.8 kΩ, 11.8 V input, synchro or resolver.
For DDC-49590: Ri = 270 kΩ, 90 V input, synchro or resolver.
Maximum addition error is 1 LSB.

**FIGURE 10B. DIFFERENTIAL RESOLVER INPUT, USING DDC-49530 (11.8 V) OR DDC-49590 (90 V)**

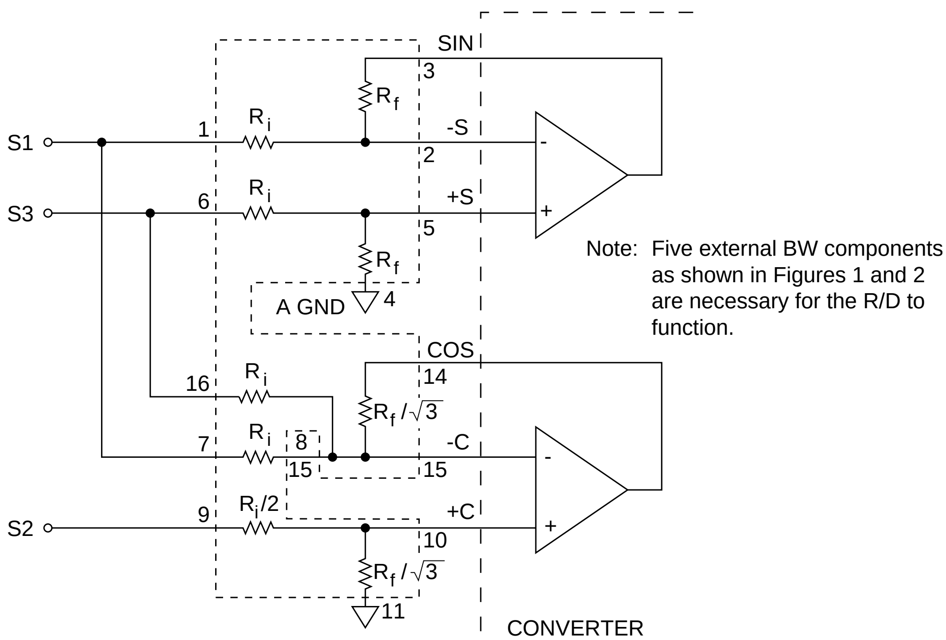



$\frac{Ri}{Rf}$ X 2 Vrms = Resolver L-L rms voltage

Rf ≥ 6 kΩ

S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded,
In both cases the shield should be tied to AGND at the converter.

**FIGURE 10C. SYNCHRO INPUT**




S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded,
In both cases the shield should be tied to AGND at the converter.
90 V input = DDC-49590: Ri = 270 kΩ, 90 V input, synchro or resolver.
11.8 V input = DDC-49530: Ri = 70.8 kΩ, 11.8 V input, synchro or resolver.
Maximum addition error is 1 LSB.

**FIGURE 10D. SYNCHRO INPUT, USING DDC-49530 (11.8 V) OR DDC-49590 (90 V)**

## DC INPUTS

As noted in TABLE 1 the RDC-19220/2S will accept DC inputs. It is necessary to set the REF input to DC by tying +REF to +5 V and -REF to GND or -5 V. (With DC inputs, the $\overline{\text{BIT}}$ output is not valid.)

## VELOCITY TRIMMING

RDC-19220/2S specifications for velocity scaling, reversal error, and offset are contained in TABLE 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. FIGURE 11 shows the setup for trimming these parameters with external potentiometers. It should also be noted that when the resolution is changed, velocity scaling is also changed. Since the VEL output is from an integrator with capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

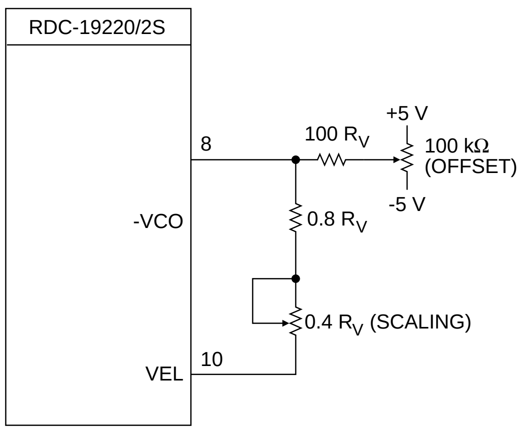



FIGURE 11. VELOCITY TRIMMING

## SYNTHESIZED REFERENCE

The synthesized reference section of the RDC-19220/2S eliminates errors caused by quadrature voltage which is due to a phase shift between the reference and the signal lines. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their signals lead the reference signal (RH and RL) by about 6°.

When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. As shown in FIGURE 1, the converter synthesizes its own $\cos(\omega t + \alpha)$ reference signal from the $\sin\theta \cos(\omega t + \alpha)$, $\cos\theta - \cos(\omega t + \theta)$ signal inputs and from the $\cos\omega t$ reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be reduced. The synthesized reference circuit also eliminates the 180° false error null hang up.

Due to the inductive nature of resolvers, the output signals typically lead the reference by 6°, and a 6° phase shift will cause problems for a 1.3 / 2.3 arc minute accuracy converter. A synthesized reference will always be exactly in phase with the signal input.

## LVDT (LINEAR VARIABLE DIFFERENTIAL TRANSFORMER) MODE

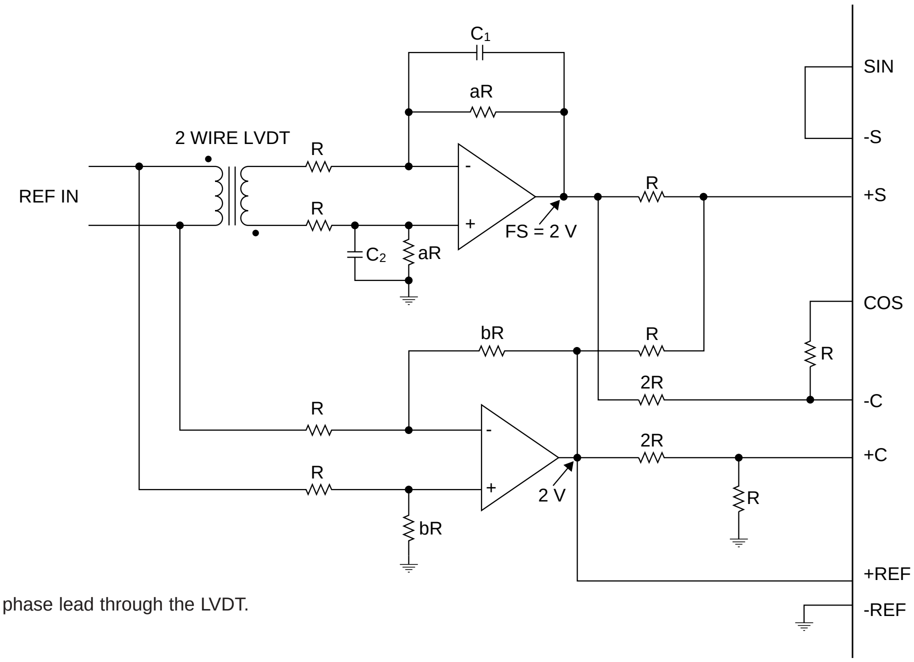
As shown in TABLE 1 the RDC-19220/2S unit can be made to operate as a LVDT-to-digital converter by connecting Resolution Control inputs A and B to "0," "1," or the -5 volt supply. In this mode the RDC-19220/2S functions as a ratiometric tracking linear converter. When linear AC inputs are applied from an LVDT the converter operates over one quarter of its range. This results in two less bits of resolution for LVDT mode than are provided in resolver mode.

The LVDT output signals will need to be scaled to be compatible with the converter input. FIGURE 12B is a schematic of an input scaling circuit applicable to 3-wire LVDTs. The value of the scaling constant "a" is selected to provide an input of 2 Vrms at full stroke of the LVDT. The value of scaling constant "b" is selected to provide an input of 1 Vrms at null of the LVDT. Suggested components for implementing the input scaling circuit are a quad op-amp, such as a 4741 type, and precision thin-film resistors of 0.1% tolerance. FIGURE 12A illustrates a 2-wire LVDT configuration.

Data output of the RDC-19220/2S is Binary Coded in LVDT mode. The most negative stroke of the LVDT is represented by ALL ZEROS and the most positive stroke of the LVDT is represented by ALL ONES. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code "01" and negative overrange is indicated by code "11" (see TABLE 6).

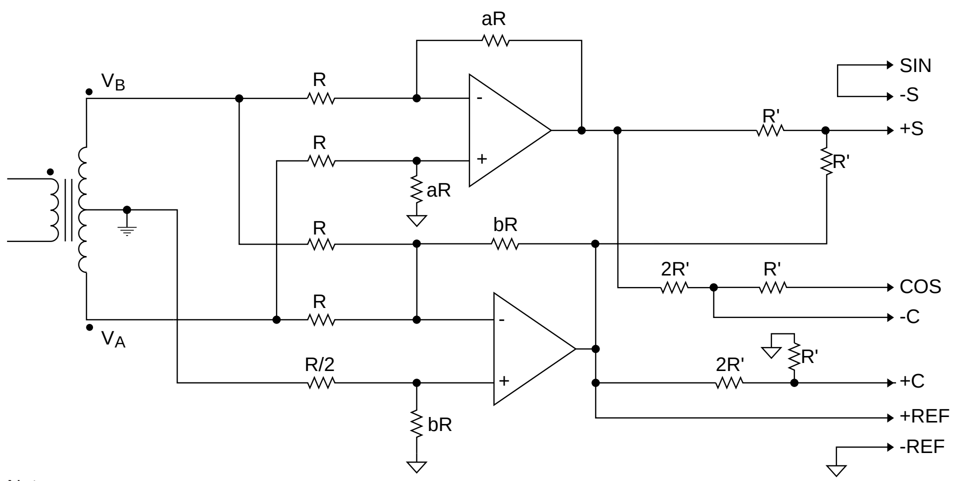
TABLE 6. 12-BIT LVDT OUTPUT CODE FOR FIGURE 12B

| LVDT OUTPUT | MSB | | | LSB |
|---|---|---|---|---|
| + over full travel | 01 | xxxx | xxxx | xxxx |
| + full travel -1 LSB | 00 | 1111 | 1111 | 1111 |
| +0.5 travel | 00 | 1100 | 0000 | 0000 |
| +1 LSB | 00 | 1000 | 0000 | 0001 |
| null | 00 | 1000 | 0000 | 0000 |
| - 1 LSB | 00 | 0111 | 1111 | 1111 |
| -0.5 travel | 00 | 0100 | 0000 | 0000 |
| - full travel | 00 | 0000 | 0000 | 0000 |
| - over full travel | 11 | xxxx | xxxx | xxxx |



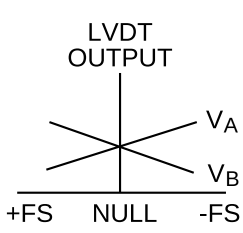

C1 = C2, set for phase lag = phase lead through the LVDT.

## FIGURE 12A. 2-WIRE LVDT DIRECT INPUT




Notes:

1. R' ≥ 10 kΩ
2. Consideration for the value of R is LVDT loading.
3. RMS values given.

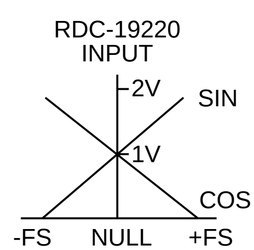



$$b = \frac{1}{V_{Anull}} = \frac{1}{V_{Bnull}}$$

$$a = \frac{2}{(V_A - V_B)_{max}}$$

$$SIN = 1 + \frac{a}{2}(V_A - V_B)$$

$$COS = 1 - \frac{a}{2}(V_A - V_B)$$




## FIGURE 12B. 3-WIRE LVDT SCALING CIRCUIT

## INHIBIT, ENABLE, AND CB TIMING

The Inhibit ($\overline{\text{INH}}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 13, angular output data is valid 150 ns maximum after the application of the negative inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{\text{EM}}$) is used for the most significant 8 bits and Enable LSBs ($\overline{\text{EL}}$) is used for the least significant 8 bits. As shown in FIGURE 14, output data is valid 150 ns maximum after the application of a negative enable pulse. The tri-state data bus returns to the high impedance state 100 ns maximum after the rising edge of the enable signal.

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB. As shown in FIGURE 15, output data is valid 50 ns maximum after the middle of the CB pulse. The CB pulse width is 1/40 Fs, which is nominally 375 ns.

## BUILT-IN-TEST ($\overline{\text{BIT}}$)

The Built-In-Test output ($\overline{\text{BIT}}$) monitors the level of error from the demodulator. This signal is the difference in the input and output angles and ideally should be zero; if it exceeds approximately 100 LSBs (of the selected resolution) the logic level at $\overline{\text{BIT}}$ will change from a logic 1 to a logic 0.

This condition will occur during a large step and reset after the converter settles out. $\overline{\text{BIT}}$ will also change to logic 0 for an over-velocity condition, because the converter loop cannot maintain input-output or if the converter malfunctions where it cannot maintain the loop at a null. $\overline{\text{BIT}}$ will also be set low for a detected Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR). The $\overline{\text{BIT}}$ signal may pulse during certain error conditions, i.e., when the converter is in a spin around condition or the signal amplitude is on the threshold of LOS.

LOS will be detected if both sin and cos input voltages are less than 500 mV peak. LOR will be detected if the differential reference voltage is less than 500 mV peak.

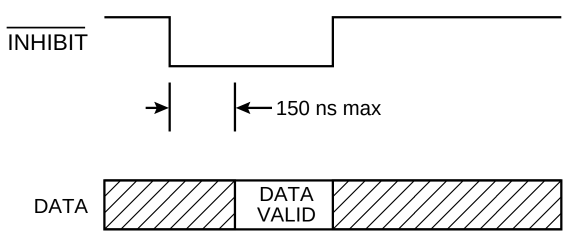



FIGURE 13. INHIBIT TIMING

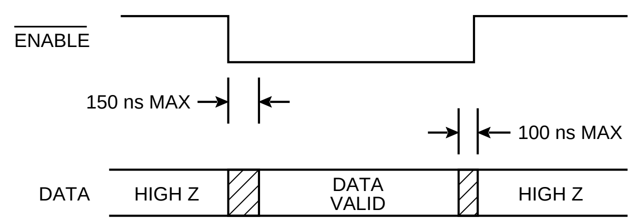



FIGURE 14. ENABLE TIMING

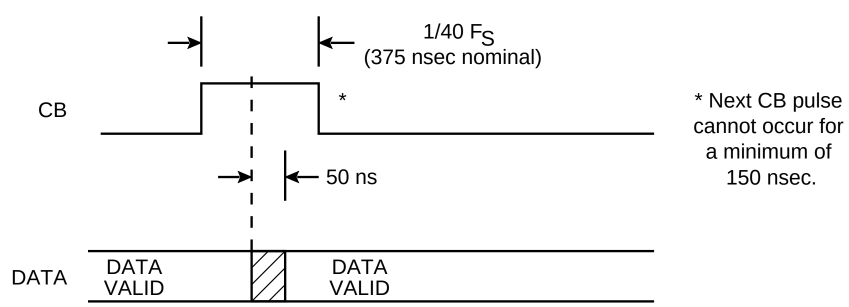



FIGURE 15. CONVERTER BUSY TIMING

## PIN OUT FUNCTION TABLES BY MODEL NUMBER

The following tables detail pin out functions by the DDC model number.

The RDC-19220S has differential inputs but requires both ±5 V power supplies.

The RDC-19222S has differential inputs and can be used with ±5 V or +5 V only.

**TABLE 7. RDC-19220S (40-PIN) PIN OUTS**

| # | NAME | DESCRIPTION | # | NAME | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | A | Resolution Control | 40 | +5 V | Power Supply |
| 2 | B | Resolution Control | 39 | $\overline{EL}$ | Enable LSBs |
| 3 | $\overline{INH}$ | Inhibit | 38 | Bit 16 | LSB |
| 4 | +REF | +Reference Input | 37 | Bit 8 | |
| 5 | -REF | -Reference Input | 36 | Bit 15 | |
| 6 | -VCO | Neg. VCO Input | 35 | Bit 7 | |
| 7 | -VSUM | Vel Sum Point | 34 | Bit 14 | |
| 8 | VEL | Velocity Output | 33 | Bit 6 | |
| 9 | +C | Signal Input | 32 | Bit 13 | |
| 10 | COS | Signal Input | 31 | Bit 5 | |
| 11 | -C | Signal Input | 30 | Bit 12 | |
| 12 | +S | Signal Input | 29 | Bit 4 | |
| 13 | +SIN | Signal Input | 28 | Bit 11 | |
| 14 | -S | Signal Input | 27 | Bit 3 | |
| 15 | -5 V | Power Supply | 26 | Bit 10 | |
| 16 | $R_S$ | Sampling Set | 25 | Bit 2 | |
| 17 | $R_C$ | Current Set | 24 | Bit 9 | |
| 18 | $\overline{EM}$ | Enable MSBs | 23 | Bit 1 | MSB |
| 19 | A GND | Analog Ground | 22 | CB | Converter Busy |
| 20 | GND | Ground | 21 | $\overline{BIT}$ | Built-In-Test |

**TABLE 8. RDC-19222S (44-PIN) PIN OUTS**

| # | NAME | DESCRIPTION | # | NAME | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | $\overline{EL}$ | Enable LSBs | 44 | BIT 16 | LSB |
| 2 | +5V | Power Supply (see note) | 43 | BIT 8 | |
| 3 | A | Resolution Control | 42 | Bit 15 | |
| 4 | B | Resolution Control | 41 | Bit 7 | |
| 5 | $\overline{INH}$ | Inhibit | 40 | Bit 14 | |
| 6 | +REF | +Reference Input | 39 | Bit 6 | |
| 7 | -REF | -Reference Input | 38 | Bit 13 | |
| 8 | -VCO | Neg. VCO Input | 37 | Bit 5 | |
| 9 | -VSUM | Vel Sum Point | 36 | Bit 12 | |
| 10 | VEL | Velocity Output | 35 | Bit 4 | |
| 11 | +C | Signal Input | 34 | Bit 11 | |
| 12 | COS | Signal Input | 33 | Bit 3 | |
| 13 | -C | Signal Input | 32 | Bit 10 | |
| 14 | +S | Signal Input | 31 | Bit 2 | |
| 15 | SIN | Signal Input | 30 | Bit 9 | |
| 16 | -S | Signal Input | 29 | Bit 1 | MSB |
| 17 | -5V | Power Supply | 28 | CB | Converter Busy |
| 18 | $R_S$ | Sampling Set | 27 | $\overline{BIT}$ | Built-in-Test |
| 19 | $R_C$ | Current Set | 26 | +5C (+5V) | Pos. Supply Cap |
| 20 | $\overline{EM}$ | Enable MSBs | 25 | +CAP | Pos. Terminal |
| 21 | A GND | Analog Ground | 24 | GND | Ground |
| 22 | -5C (-5V) | Neg. Supply Cap | 23 | -CAP | Neg. Terminal |

**Note:** When using the built-in -5 V inverter: connect pin 2 to 26, pin 17 to 22, and a 10 µF/10 VDC capacitor from pin 23 (negative terminal) to pin 25 (positive terminal). Connect a 47 µF/10 VDC capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed.

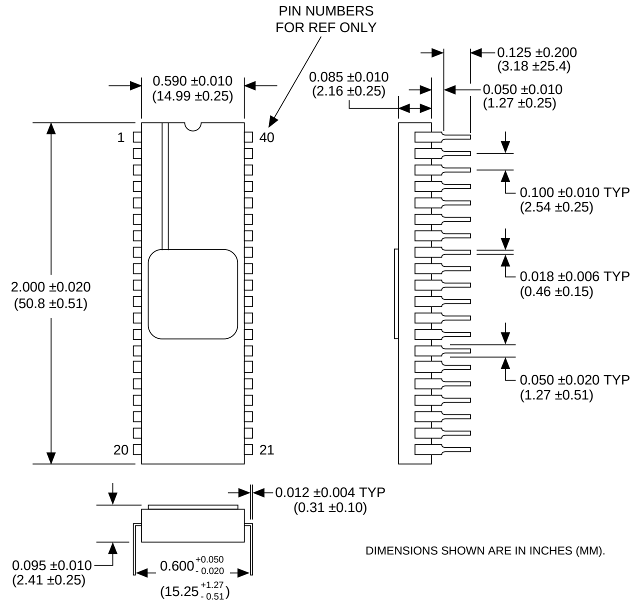



**FIGURE 16. RDC-19220S (40-PIN DDIP) CERAMIC PACKAGE MECHANICAL OUTLINE**

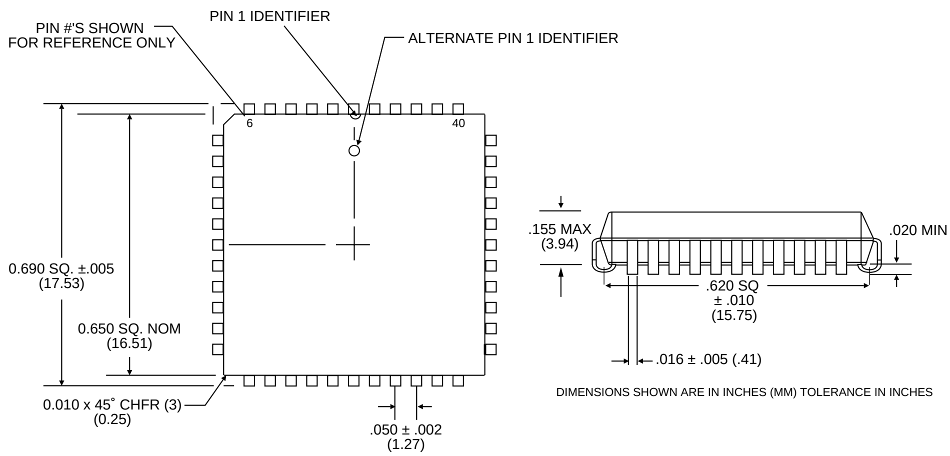



**FIGURE 17. RDC-19222S (44-PIN PLASTIC J-LEAD) MECHANICAL OUTLINE**

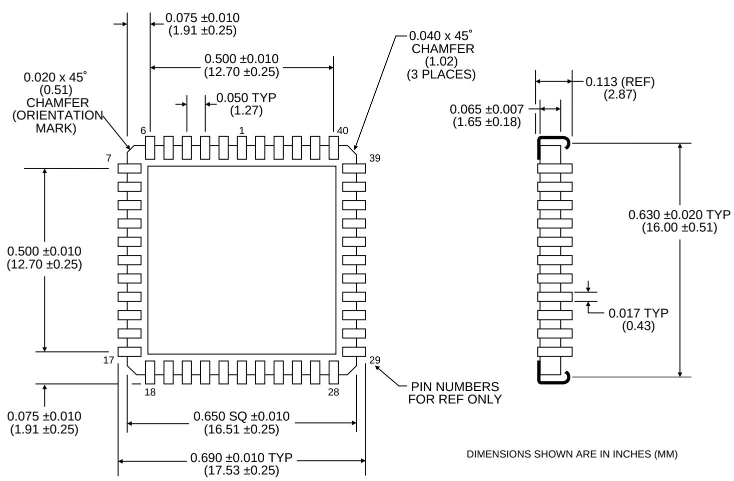



**FIGURE 18. RDC-19222S (44-PIN CERAMIC J-LEAD) MECHANICAL OUTLINE**

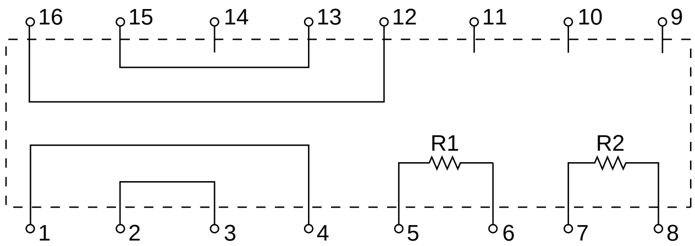



**FIGURE 19. (DDC-55688-1) LAYOUT AND RESISTOR VALUES (R1 AND R2 = 10 KΩ 1.0% TOL, ABSOLUTE TC = ±100 PPM MAX)**

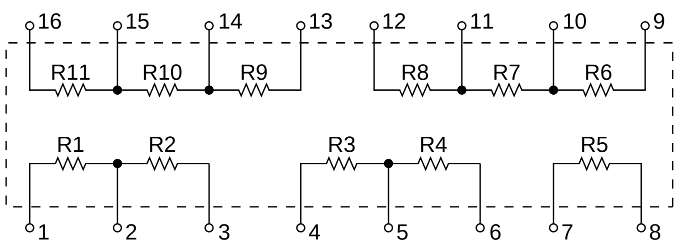



**FIGURE 20. (DDC-49530, DDC-49590, DDC-57470) LAYOUT AND RESISTOR VALUES (SEE TABLE 9)**

**TABLE 9. FRONT-END THIN-FILM RESISTOR NETWORKS (SEE FIGURE 20)**

| DDC-49530, DDC-57470 RESISTOR VALUES (11.8 V INPUTS) | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOL | ABS VALUE (Ω) | TOL (%) | REL TO | REL VALUE (Ω) | TOL (%) | TCR(PPM) |
| R1 | 70.8 k | 0.1 | | | | 25 |
| R2 | | | R1 | 12 k | 0.02 | 2 |
| R3 | | | R4 | 12 k | 0.02 | 2 |
| R4 | | | R1 | 70.8 k | 0.02 | 2 |
| R5 | | | R1 | 70.8 k | 0.02 | 2 |
| R6 | | | R1 | 35.4 k | 0.02 | 2 |
| R7 | | | R6 | 6.9282 k | 0.02 | 2 |
| R8 | | | R6 | 5.0718 k | 0.02 | 2 |
| R9 | | | R11 | 5.0718 k | 0.02 | 2 |
| R10 | | | R11 | 6.9282 k | 0.02 | 2 |
| R11 | | | R1 | 70.8 k | 0.02 | 2 |
| **DDC-49590 RESISTOR VALUES (90 V INPUTS)** | | | | | | |
| R1 | 270 k | 0.1 | | | | 25 |
| R2 | | | R1 | 6 k | 0.02 | 2 |
| R3 | | | R4 | 6 k | 0.02 | 2 |
| R4 | | | R1 | 270 k | 0.02 | 2 |
| R5 | | | R1 | 270 k | 0.02 | 2 |
| R6 | | | R1 | 135 k | 0.02 | 2 |
| R7 | | | R6 | 3.4641 k | 0.02 | 2 |
| R8 | | | R6 | 2.5359 k | 0.02 | 2 |
| R9 | | | R11 | 2.5359 k | 0.02 | 2 |
| R10 | | | R11 | 3.4641 k | 0.02 | 2 |
| R11 | | | R1 | 270 k | 0.02 | 2 |

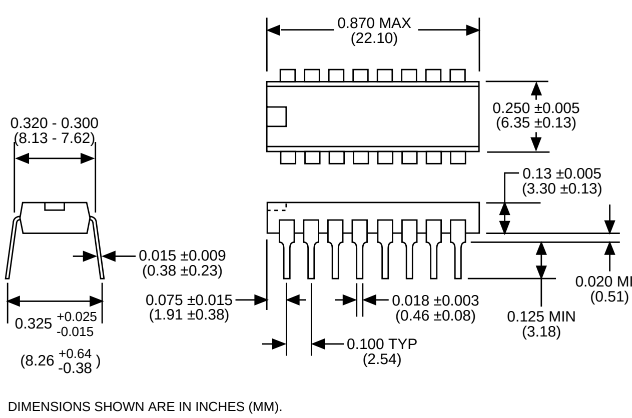



**FIGURE 21. 16-PIN THIN-FILM RESISTOR NETWORK DIP MECHANICAL OUTLINE (DDC-49530, DDC-55688-1)**

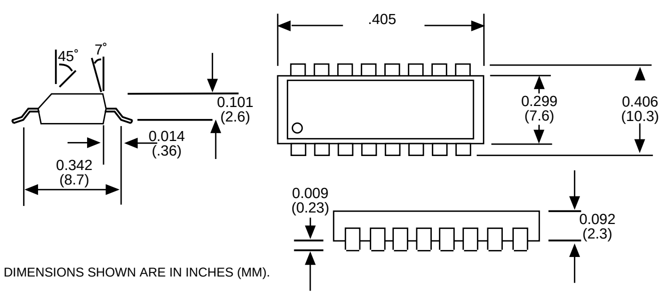



**FIGURE 22. 16-PIN THIN-FILM RESISTOR NETWORK FLAT-PACK MECHANICAL OUTLINE (DDC-57470)**

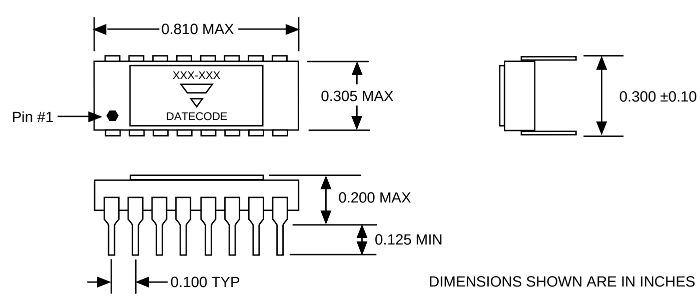



**FIGURE 23. 16-PIN THIN-FILM RESISTOR NETWORK DIP MECHANICAL OUTLINE - CERAMIC PACKAGE (DDC-49590)**

## ORDERING INFORMATION

**RDC-19222S - XXXX** **(Plastic Package: 44-pin J-Lead)**

**Supplemental Process Requirements:**
T = Tape and Reel
Blank = None of the Above

**Accuracy:**
2 = 4 minutes + 1 LSB
3 = 2 minutes + 1 LSB
5 = 1 minute + 1 LSB (maximum reference frequency = 5kHz)

**Process Requirements:**
0 = No Burn-In
9 = Solder Dip, without Burn-In

**Temperature Grade:**
2 = -40 to +85°C
3 = 0 to +70°C

**RDC-1922XS - XXXX** **(Ceramic Package)**

**Supplemental Process Requirements:**
T = Tape and Reel (Not available in 40-pin DDIP package)
S = Pre-Cap Source Inspection
L = 100% Pull Test
Q = Pre-Cap Source and 100% Pull Test
K = One Lot Date Code
W = One Lot Date Code and Pre-Cap Source Inspection
Y = One Lot Date Code and 100% Pull Test
Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test
Blank = None of the Above

**Accuracy:**
3 = 2 minutes + 1 LSB

**Process Requirements:**
0 = Standard DDC Processing, without Burn-In
1 = MIL-PRF-38534 Compliant
2 = Standard DDC Processing, with Burn-In
3 = MIL-PRF-38534 Compliant, with PIND testing
4 = MIL-PRF-38534 Compliant, with Solder Dip
5 = MIL-PRF-38534 Compliant, with PIND testing, and Solder Dip
6 = Standard DDC Processing, with PIND testing, and Burn-In
7 = Standard DDC Processing, with Solder Dip, and Burn-In
9 = Standard DDC Processing, with Solder Dip, without Burn-In

**Temperature Grade / Data Requirements:**
1 = -55 to +125°C
4 = -55 to +125°C, with Variables Test Data

**Package:**
0 = 40-Pin DDIP, (“+5 volt only” power supply feature - not available)
2 = 44-Pin J-Lead

**STANDARD DDC PROCESSING**

| TEST | MIL-STD-883 | |
|---|---|---|
| | METHOD(S) | CONDITION(S) |
| INSPECTION | 2009, 2017 | — |
| SEAL | 1014 | A and C |
| TEMPERATURE CYCLE | 1010 | C |
| CONSTANT ACCELERATION | 2001 | 3000g |
| BURN-IN | 1015, Table 1 | — |

## ORDERING INFORMATION (CONTINUED)

**RDC-19229S - 4XXX** **(Class K Processed Part Ordering Information)**

**Mandatory Process Requirements Selection: (One of the following must be selected)**
- L = 100% Pull Test
- Q = Pre-Cap Source and 100% Pull Test (Contact factory for availability)
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source Inspection and 100% Pull Test (Contact factory for availability)

**Accuracy:**
- 3 = 2 minutes + 1 LSB

**Process Requirements: (Burn-In is in accordance with MIL-STD-883 Class K)**
- 6 = 320 hour Burn-In at +125°C, with PIND testing
- 8 = 320 hour Burn-In at +125°C, with PIND testing and Solder Dip

**Temperature Grade / Data Requirements:**
- 4 = -55 to +125°C, with Variables Test Data

**Package:**
- 9 = Screened to Class K, 44-Pin J-Lead ceramic package

**THIN-FILM RESISTOR NETWORKS: (Operating temperature range: -55 to +125°C)**

DDC-49530 = 11.8 V input, DIP
DDC-57470 = 11.8 V input, surface mount
DDC-49590 = 90 V input, DIP
DDC-55688-1 = 2 V direct, DIP

External Component Selection Software (refer to General Setup Conditions section) can be downloaded from DDC's web site: www.ddc-web.com.

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